REMARKS

I. Introduction

In response to the Office Action August 14, 2006, Applicant has amended claim 14 to further clarify the subject matter of the present invention. Support for the amendment to claim 14 may be found, for example, on page 21, lines 22-23 of the specification. No new matter has been added.

For the reasons set forth below, Applicant respectfully submits that all pending claims are patentable over the cited prior art references.

II. The Rejection Of Claims 14, 15, 17 And 18 Under 35 U.S.C. § 103

Claims 14, 15, 17 and 18 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Ahn (USP No. 6,110,771) in view of Matsuoka et al. (USP No. 6,333,541) and Shepela et al. (USP No. 6,060,387). Applicant respectfully traverses this rejection for at least the following reasons.

With regard to the present invention, amended claim 14 recites, a semiconductor device comprising a MOS transistor with a plurality of gate electrodes, wherein the gate electrodes are formed on a semiconductor substrate having a silicon layer at least in the surface thereof, the MOS transistor has a gate length of 0.15 μm or smaller and is formed in an element region surrounded with an isolation insulating film, each of the gate electrodes is arranged between dummy patterns with a space left from each side thereof, sidewalls are provided on side walls of each of the gate electrodes, a first silicide layer is formed in the upper portion of the gate electrode, a second silicide layer is formed in a portion of the semiconductor substrate surface which is located in part of the element region between the gate electrode and the dummy

patterns, the first silicide layer has a greater thickness than the second silicide layer, one of the dummy patterns is a dummy gate electrode which is an electrode pattern having the shape of a gate electrode, and the other dummy pattern is a pattern made of insulating material, and the dummy patterns are formed on the isolation insulating film.

It was alleged in the Office Action that Ahn teaches, in col. 3, lines 35-59, that one of the dummy patterns is a dummy gate electrode 124c which is an electrode pattern having the shape of a gate electrode, and the other dummy pattern is a pattern made of insulating material 123. However, Ahn teaches "...and the other region of the semiconductor substrate 121 is an active region on which an gate oxide film 123 is formed" (col. 3, lines 39-41). Nowhere in this passage does Ahn disclose that both of the gate oxide film 123 and the dummy gate electrode 124c constitute a part of the dummy patterns. Accordingly, Ahn fails to disclose that one of the dummy patterns is a dummy gate electrode which is an electrode pattern having the shape of a gate electrode.

In addition, Ahn teaches that the gate oxide films 123, 205 are provided on the active regions in the semiconductor substrate (see, col. 3, lines 39-41 of Ahn) and the dummy gate electrodes 124c, 206c are provided on the first impurity layer 127 (see, col. 4, lines 10-14 of Ahn). Thus, even if the gate oxide film 123 could be interpreted as a dummy pattern, Ahn fails to disclose that the dummy patterns are formed on the isolation insulating film. In contrast to Ahn, the present invention discloses that the dummy patterns are formed on the isolation insulating film. As can be seen, for example, in Fig. 9D and page 22, lines 22-27 of the present invention, the insulating layer is formed by CVD on the entire surface above the semiconductor substrate 30, forming the dummy patterns 31 made of insulating material and also,

simultaneously, the insulating material 33 is formed on the resistance portion 32 and the sidewalls 4 in contact with the resistance portion, all on the isolation insulating film 1.

As such, Ahn fails to disclose a semiconductor device wherein one of the dummy patterns is a dummy gate electrode which is an electrode pattern having the shape of a gate electrode, and the other dummy pattern is a pattern made of insulating material, and the dummy patterns are formed on the isolation insulating film. Moreover, Matsuoka and Shepela both fail to remedy this deficiency.

In order to establish *prima facie* obviousness of a claimed invention, all the claim limitations must be taught or suggested by the prior art. *In re Royka*, 180 USPQ 580 (CCPA1974). As Ahn, Matsuoka and Shepela, at a minimum, fail to describe a semiconductor device wherein one of the dummy patterns is a dummy gate electrode which is an electrode pattern having the shape of a gate electrode, and the other dummy pattern is a pattern made of insulating material, and the dummy patterns are formed on the isolation insulating film, it is submitted that Ahn, alone or in combination with Matsuoka and Shepela, does not render claim 14 obvious. Accordingly, it is respectfully requested that the § 103 rejection of claim 14, and any pending claims dependent thereon be withdrawn.

III. All Dependent Claims Are Allowable Because The Independent Claim From Which They Depend Is Allowable

Under Federal Circuit guidelines, a dependent claim is nonobvious if the independent claim upon which it depends is allowable because all the limitations of the independent claim are contained in the dependent claims, *Hartness International Inc. v. Simplimatic Engineering Co.*, 819 F.2d at 1100, 1108 (Fed. Cir. 1987). Accordingly, as claim 14 is patentable for the reasons

set forth above, it is respectfully submitted that all pending dependent claims are also in condition for allowance.

IV. Conclusion

Having fully responded to all matters raised in the Office Action, Applicant submits that all claims are in condition for allowance, an indication of which is respectfully solicited.

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,

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